# BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

## IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.**

# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/779,351 | 02/12/2004 | B. Arlen Young | ADPT105102 | 9600 |

23513 7590 07/14/2004

GUNNISON MCKAY & HODGSON, LLP
GARDEN WEST OFFICE PLAZA, SUITE 220
1900 GARDEN ROAD
MONTEREY, CA 93940

| EXAMINER | |
|---|---|
| NGUYEN, TANH Q | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2182 | |

DATE MAILED: 07/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/779,351 | YOUNG, B. ARLEN | |
| | Examiner | Art Unit | |
| | Tanh Q. Nguyen | 2182 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *20 and 22-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20 and 22-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. The current status of all nonprovisional parent applications and serial number of the copending divisional applications referenced should be included.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claims 20, 22-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 25 recites the limitation "as in Claim 18" in line 2.

Claim 26 recites the limitation "as in Claim 18" in line 2.

There is insufficient antecedent basis for the limitation in claims 25 and 26 - as claim 18 is cancelled. Since claims 25-26 recite limitations similar to those of claims 32-33 - which depend on independent claim 27, claims 25-26 are best interpreted as being dependent on independent claim 20.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 20, 22-33 are rejected under 35 U.S.C. 102 (e) as being anticipated by **Arnon et al. (USP 6,321,308)**.

7. As per claims 20, 27, **Arnon** teaches a system [FIG. 1 and FIG. 2] comprising:

a host adapter [22a, 22b, 22n, 23, FIG. 2];

a plurality of target devices [28a-e, 14, 15, FIG. 2; 14, 16, FIG. 1] coupled to said host adapter; and

a memory [27, FIG. 2] coupled to said host adapter, and said memory having stored therein a hardware I/O control block memory array [30, FIG. 3; col. 4, lines 33-44] comprising:

a first hardware I/O control block [32, FIG. 3] having a sister hardware control block field [NEXT RECORD PTR 48, Fig. 3]; and

a second hardware I/O control block [38, FIG. 3] having a sister hardware I/O control block field [NEXT RECORD PTR 42, Fig. 3] wherein said sister hardware I/O control block field of said second hardware I/O control block includes a pointer [42, FIG. 3] to said first hardware I/O control block [32, FIG. 3] wherein said first and second hardware I/O control blocks are used for a mirrored data transaction using at least two target devices in said plurality of target devices (col. 3, lines 33-36).

Arnon does not explicitly teach the sister hardware I/O control block field of the first hardware I/O control block including a pointer to the second hardware I/O control block. Arnon, however, teaches deletion of hardware I/O control block [34, FIG. 4; col. 7, lines 50-63] from the hardware I/O control block memory array by replacing the pointer in the sister hardware control block field of the first hardware I/O control block [48, FIG. 3] with a pointer [51, FIG. 4] to hardware I/O control block [36, FIG. 4], hence implicitly teaches that when the hardware I/O control block memory array comprises only the first and second hardware I/O control blocks (as when hardware I/O control blocks 34 and 36 of FIG. 3 are deleted), the sister hardware I/O control block field of the first hardware I/O control block includes a pointer to the second hardware I/O control block.

8. As per claims 22-24, 28-31, Arnon teaches that upon completion of execution of a hardware I/O control block, the hardware I/O control block is deleted (col. 5, lines 45-47), and the pointer to a deleted hardware I/O control block being no longer valid [FIG. 4; col. 63-65 - pointer 48 no longer exists after deletion of 34), hence implicitly teaches that when the hardware I/O control block memory array comprises only the first and second hardware I/O control blocks, and

when the pointer in the sister field of the first hardware I/O command block is a valid pointer upon completion of execution of said first hardware I/O control block, the sister field of said second hardware I/O control block is changed to an invalid pointer (i.e. a null pointer), hence a null identification number - as upon deletion of the first hardware I/O command block, only the second hardware I/O command block remains in

the hardware I/O control block memory array and the NEXT RECORD PTR of the second hardware I/O command block would therefore be a null pointer;

when the pointer in the sister field of the second hardware I/O command block is a valid pointer upon completion of execution of said second hardware I/O control block, the sister field of said first hardware I/O control block is changed to an invalid pointer (i.e. a null pointer), hence a null identification number - as upon deletion of the second hardware I/O command block, only the first hardware I/O command block remains in the hardware I/O control block memory array and the NEXT RECORD PTR of the first hardware I/O command block would therefore be a null pointer.

9. As per claims 25-26, 32-33, Arnon teaches a mirrored data transaction comprising a read transaction and a write transaction (col. 3, lines 33-40; col. 4, lines 1-22).

10. As per claims 20, 25-27, 32-33, Arnon alternatively teaches a system [FIG. 1 and FIG. 2] comprising:

a host adapter [22a, 22b, 22n, 23, FIG. 2];

a plurality of target devices [28a-e, 14, 15, FIG. 2; 14, 16, FIG. 1] coupled to said host adapter; and

a memory [27, FIG. 2] coupled to said host adapter, and said memory having stored therein a hardware I/O control block memory array [30, FIG. 3; col. 4, lines 33-44] comprising:

a first hardware I/O control block [32, FIG. 3] having a sister hardware control

block field [NEXT RECORD PTR 48, Fig. 3]; and

a second hardware I/O control block [34, FIG. 3] having a sister hardware I/O control block field [PREVIOUS RECORD PTR 46, Fig. 3] wherein the sister hardware I/O control block field of the first hardware I/O control block includes a pointer [48, FIG. 3] to the second hardware I/O control block and the sister hardware I/O control block field of said second hardware I/O control block includes a pointer [46, FIG. 3] to the first hardware I/O control block [32, FIG. 3] wherein the first and second hardware I/O control blocks are used for a mirrored data transaction using at least two target devices in said plurality of target devices (col. 3, lines 33-36).

Arnon further teaches a mirrored data transaction comprising a read transaction and a write transaction (col. 3, lines 33-40; col. 4, lines 1-22).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (703) 305-0138, and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 for After Final, Official, and Customer Services, or (703) 746-5672 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

Mail Stop ____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Effective December 1, 2003, hand-carried patent application related incoming correspondences will be to a centralized location.

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TQN
July 8, 2004